REMARKS

INTRODUCTION

In accordance with the foregoing, the specification, no claims have been amended. Claims 16 and 28 have been cancelled without prejudice to or disclaimer of the subject matter disclosed therein. Claims 1-15, 17-27 and 29-38 are pending and under consideration.

CLAIM REJECTIONS - 35 USC §102

In the Office Action at page 7, numbered paragraph 8, claims 1-13, 19-24, 27-31 and 33-37 were rejected under 35 USC §102(e) as being anticipated by Owa et al. (US 6,564,009) (hereinafter, "Owa"). Applicant respectfully traverses this rejection.

Owa discloses an optical disk recording and/or reproducing apparatus that increases a record density of the disk by rotating the disk in such a manner that the R/W CK is constant so that the line record density does not change significantly between the inner periphery and outer periphery of the disk. Owa further discloses that wobble data address in pre-groove (ADIP) may be decoded by detecting a phase change of the wobble signal. Owa further discloses that by comparing a binarized version of the wobble signal WB (data) 39 with a CK, having a frequency twice that of the binarized wobble signal, a result of the phase comparison may control an oscillation frequency of a voltage type oscillating circuit (VCO). Thus, in the PLL circuit 135, the frequency output by the VCO may be increased more than the frequency of the wobble signal WB (i.e., data) in steps in accordance with a displacement position of the laser beam to the outer peripheral side of the disk 12, and that the oscillation output may be a constant frequency R/W CK. Owa, column 15, lines 7-13 and column 41, lines 6-63.

Claims 1-13

Claim 1 recites: "...generating a block boundary signal indicative of a boundary between error correction code (ECC) blocks using block address information recorded on the disk; detecting a phase difference between the block boundary signal and an encoding block synchronous signal; and detecting whether a violation of the boundary occurs according to a magnitude of the detected phase difference." In contrast to claim 1, Owa does not disclose generating a boundary block signal. In Owa, a block address is detected, which is expressed by a wobble signal or a data frame, but not a boundary of blocks.

Claims 2-13 depend from claim 1 and recite patentably distinguishing features of their own.

Withdrawal of the foregoing rejection is respectfully requested.

Claims 19 and 20

Claim 19 recites: "...determining whether a violation of a block boundary occurs on a disk by determining a phase difference between a block boundary signal and an encoding block synchronous signal." In contrast to claim 19, Owa does not disclose a comparison of a block boundary signal and a synchronous signal as is recited in claim 19.

Claim 20 depends from claim 19 and recites patentably distinguishing features of its own.

Withdrawal of the foregoing rejection is respectfully requested.

Claims 21-24

Claim 21 recites: "...a decoder generating a block boundary signal showing a boundary of ECC blocks based on the block address information recorded on the disk; an encoder adding an error correction code to data provided thereto, generating an encoding block, and outputting the encoding block with an encoding block synchronous signal; and a boundary violation detector detecting a phase difference between the block boundary signal and the encoding block synchronous signal and detecting whether a violation of the boundary occurs according to a magnitude of the detected phase difference." In contrast to claim 21, Owa does not disclose comparing the place where a physical block starts on a disc with the place where ECC block data starts to be written on the disc. These places are expressed by timing pulses, such as a block boundary signal derived from the disc and a synchronous signal contained in ECC block data, respectively. As a result of the comparison, it is determined whether a block boundary is violated.

Owa discloses synchronizing the generation of ECC block data with a signal based on counting a block address. There may be inconsistency between the place where a block starts on a disc and the place where writing of ECC block data starts on the disc because operation of the disc drive may be disturbed during or after the generation of ECC block data.

Claims 22-24 depend from claim 21 and recite patentably distinguishing features of their own.

Withdrawal of the foregoing rejections is respectfully requested.

Claims 33-37

Claim 33 recites: "...a boundary violation detector determining whether a violation of a block boundary occurs on a disk by determining a phase difference between a block boundary signal and an encoding block synchronous signal." In contrast to claim 33, Owa does not disclose the determination of violation of a block boundary. Owa relates only to PLL, not to determination of violation of a block boundary. In Owa, the phase comparator 135A compares the phases of a wobble signal and a clock signal. The result of the comparison is fed to the VCO (135D) to control the frequency and phase of the clock signal. The wobble signal is not a block boundary signal as recited in claim 33, and the PLL is not used to determine whether a block boundary is violated. Comparing a block boundary signal with a synchronous signal and determining whether a block boundary is violated is not disclosed or suggested in Owa.

Claims 34-37 depend from claim 33 and recite patentably distinguishing features of their own.

Withdrawal of the foregoing rejections is respectfully requested.

CLAIM REJECTIONS - 35 USC §103.

In the Office action at page 20, numbered paragraph 9, claims 14, 25, 26 and 38 were rejected under 35 USC §103(a) as being unpatentable over Owa et al. The rejection is respectfully traversed.

Regarding claim 14, this claim is dependent on claim 1 and is believed to be allowable for at least the reasons discussed above. Regarding claims 25 and 26, these claims are dependent on claim 21 and are believed to be allowable for at least the reasons discussed above. Regarding claim 38, this claim is dependent on claim 33 and is believed to be allowable for at least the reasons discussed above.

Withdrawal of the foregoing rejections is respectfully requested.

CLAIM REJECTIONS - 35 USC §102.

In the Office action at page 21, numbered paragraph 10, claims 15, 17, 18, 27 and 29-32 were rejected under 35 USC §102(e) as being anticipated by Owa et al. in view of Ueki (US 6,678,236) (hereinafter "Ueki"). The rejection is respectfully traversed.

Ueki discloses a method and apparatus for recording information on a recording medium. Ueki further discloses that a first portion of the 1-ECC block data is recorded while the LPP-based recording timing signal is used as reference timings indicative of the boundaries between sectors or the heads of sectors. The timing corresponding to the starting edge of the pre-pit area PR and given by the LPP-based recording timing signal, the system controller 9 suspends the recording and changes the operation of the apparatus from the recording mode to the playback mode. Ueki, column 26, lines 45-55.

Claims 15, 17 and 18

Claim 15 recites: "...preventing abnormal recording on a disk recording apparatus by detecting inconsistencies between an encoding block and an error correction code block on a disk; receiving a signal from the disk and generating a block boundary signal therefrom, wherein each boundary between blocks is determined by the signal from the disk; generating a first window signal detecting whether a phase of the block boundary signal leads a phase of an encoding block synchronous signal from the encoding block..." In contrast to claim 15, neither Owa nor Ueki discloses a window signal, the window signal being used to determine lead/in phase/lag state.

Claims 17 and 18 depend from claim 15 and recite patentably distinguishing features of their own.

Withdrawal of the foregoing rejections is respectfully requested.

Claims 27 and 29-32

Claim 27 recites: "...a first logic gate comparing the encoding block synchronous signal with the first window signal and outputting a first interrupt signal; a second logic gate comparing the encoding block synchronous signal with the second window signal and outputting a second interrupt signal..." In contrast to claim 27, neither Owa nor Ueki disclose interrupt signals as recited in claim 27. Uecki discusses delaying the writing of data to skip a pre-pitted area at the beginning of a sector. However, there is no description of a delay caused by violation of a block boundary in relation to a recording/reproducing circuit of Owa, which only discusses controlling recording/reproducing speed according to bit rate. Further, there is no discussion about determining whether a clock boundary has been violated in either of the above references.

Claims 29-32 depend from claim 27 and recite patentably distinguishing features of their own.

Withdrawal of the foregoing rejections is respectfully requested.

CONCLUSION

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

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By: _____

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